AT24C04C and AT24C08C

I^2C-Compatible, (2-wire) Serial EEPROM
4-Kbit (512 x 8), 8-Kbit (1024 x 8)

DATASHEET

Standard Features

- Low-voltage and Standard-voltage Operation
  - V_{CC} = 1.7V to 5.5V
- Internally Organized as 512 x 8 (4K), or 1024 x 8 (8K)
- I^2C-compatible (2-wire) Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 1MHz (2.5V, 2.7V, 5V), 400kHz (1.7V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 16-byte Page Write Mode
  - Partial Page Writes Allowed
- Self-timed Write Cycle (5ms Max)
- High-reliability
  - Endurance: 1,000,000 Write Cycles
  - Data Retention: 100 Years
- Green Package Options (Pb/Halide-free/RoHS Compliant)
  - 8-lead PDIP, 8-lead SOIC, 8-lead TSSOP, 8-pad UDFN, 5-lead SOT23, and 8-ball VFBGA
- Die Options: Wafer Form and Tape and Reel

Description

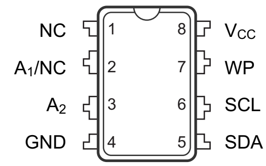
The Atmel® AT24C04C and AT24C08C provides 4,096/8,192 bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 512/1024 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. AT24C04C/08C is available in space-saving 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead TSSOP, 8-pad UDFN, 5-lead SOT23, and 8-ball VFBGA packages and is accessed via a 2-wire serial interface.

1. Pin Configurations and Pinouts

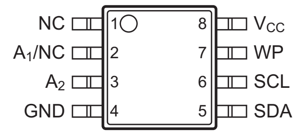
Pin Name	Function
NC	No Connect
A_1	Address Input (4K Only)
A_2	Address Input
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
GND	Ground
V_{CC}	Power Supply

Notes:
1. For use of 5-lead SOT23, the software A2 and A1 bits in the device address word must be set to zero to properly communicate.
2. Drawings are note to scale.

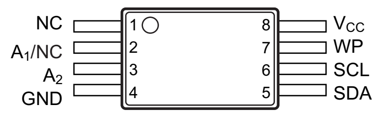
8-lead PDIP
(Top View)



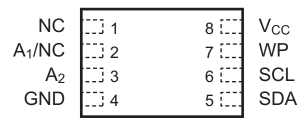
8-lead SOIC
(Top View)



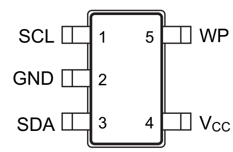
8-lead TSSOP
(Top View)



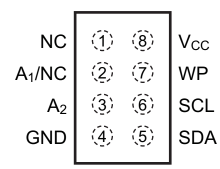
8-pad UDFN
(Top View)



5-lead SOT23
(Top View)



8-ball VFBGA
(Top View)

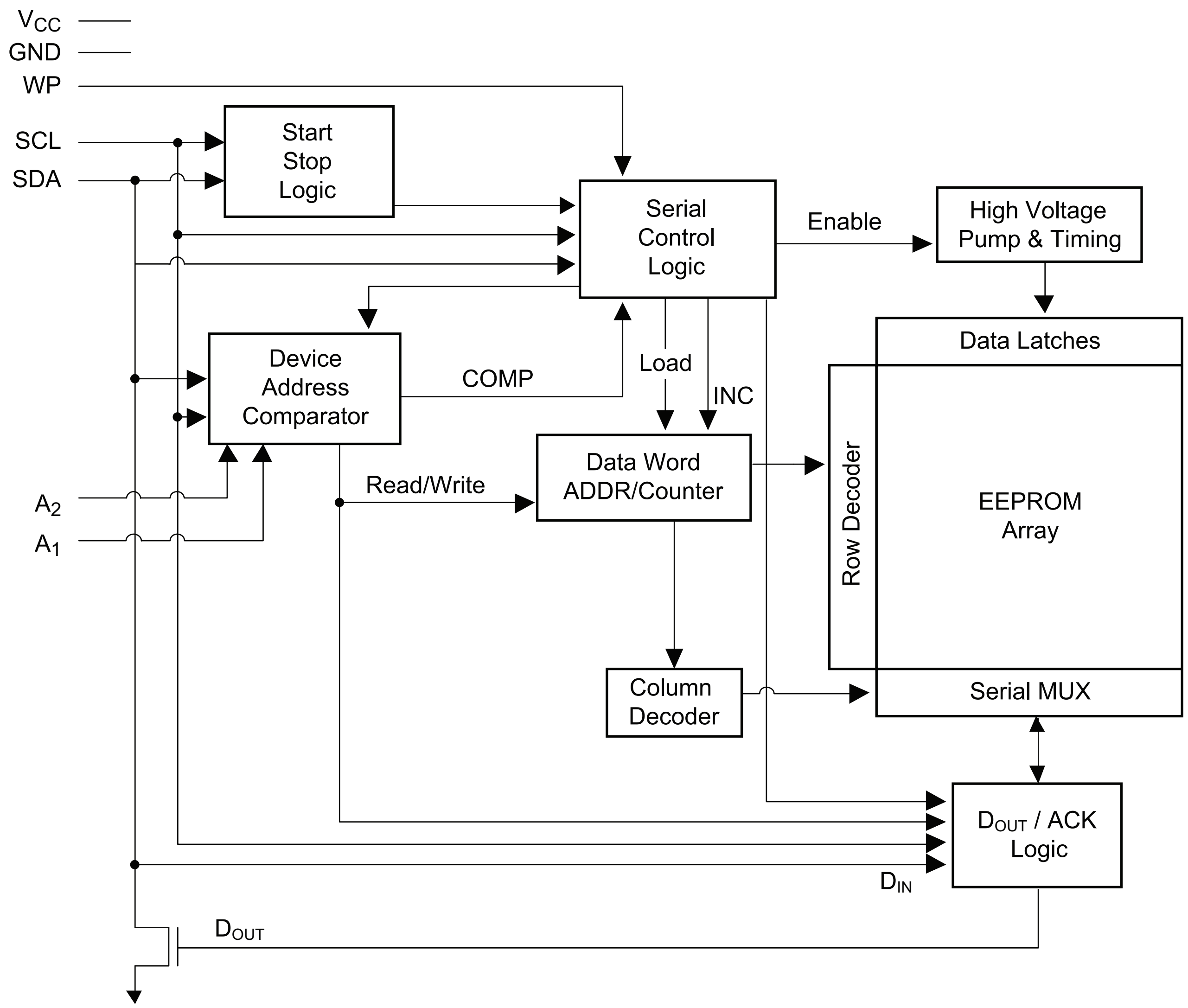


2. Absolute Maximum Ratings

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any pin with respect to ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0mA

*Notice: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3. Block Diagram



4. Pin Description

Serial Clock (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

Serial Data (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

Device/Page Addresses (A_2 and A_1): The AT24C04C uses the A_2 and A_1 inputs for hard wire addressing allowing a total of four 4K devices to be addressed on a single bus system. Pin 1 is a no connect and can be connected to ground (see Section 7. "Device Addressing" on page 10). The AT24C08C only uses the A_2 input for hardware addressing and a total of two 8K devices may be addressed on a single bus system. The A_0 and A_1 pins are no connects and can be connected to ground (see Section 7.).

Write Protect (WP): AT24C04C/08C has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to Ground (GND). When the Write Protect pin is connected to V_{CC}, the write protection feature is enabled and operates as shown in Table 4-1.

Table 4-1. Write Protect

WP Pin Status	Part of the Array Protected
At V_{CC}	Full array
At GND	Normal read/write operations

5. Memory Organization

AT24C04C, 4K Serial EEPROM: Internally organized with 32 pages of 16 bytes each, the 4K requires a 9-bit data word address for random word addressing.

AT24C08C, 8K Serial EEPROM: Internally organized with 64 pages of 16 bytes each, the 8K requires a 10-bit data word address for random word addressing.

Table 5-1. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0MHz, V_{CC} = +1.7V to +5.5V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

Table 5-2. DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.7V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		1.7		5.5	V
V_{CC2}	Supply Voltage		4.5		5.5	V
I_{CC}	Supply Current V_{CC} = 5.0V	Read at 100kHz		0.4	1.0	mA
I_{CC}	Supply Current V_{CC} = 5.0V	Write at 100kHz		2.0	3.0	mA
I_{SB1}	Standby Current V_{CC} = 1.7V	V_{IN} = V_{CC} or V_{SS}			1.0	µA
I_{SB2}	Standby Current V_{CC} = 5.5V	V_{IN} = V_{CC} or V_{SS}			6.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level[1]		-0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level V_{CC} = 3.0V	I_{OL} = 2.1mA			0.4	V
V_{OL1}	Output Low Level V_{CC} = 1.7V	I_{OL} = 0.15mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

Table 5-3. AC Characteristics

Applicable over recommended operating range from T_{AI} = -40°C to +85°C, V_{CC} = +1.7V to +5.5V, CL = 1TTL Gate and 100pF (unless otherwise noted).

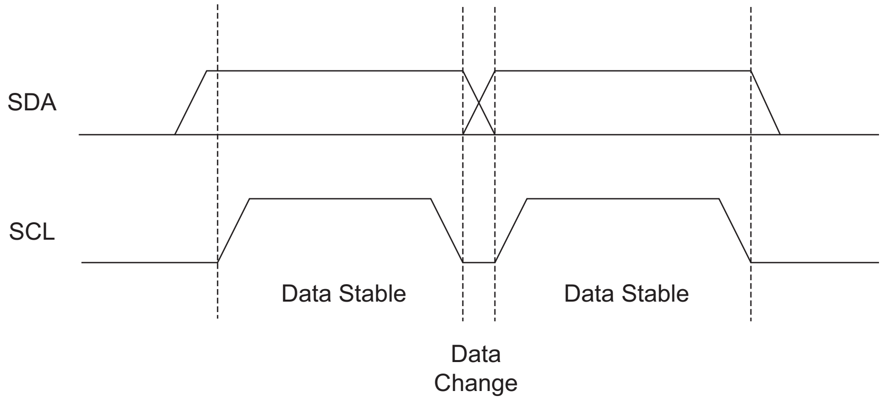
Symbol	Parameter	1.7V		2.5V, 2.7V, 5.0V		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	1.2		0.4		µs
t_{HIGH}	Clock Pulse Width High	0.6		0.4		µs
t_I	Noise Suppression Time		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	0.9	0.05	0.55	µs
t_{BUF}	Time the bus must be free before a new transmission can start.	1.2		0.5		µs
$t_{HD.STA}$	Start Hold Time	0.6		0.25		µs
$t_{SU.STA}$	Start Setup Time	0.6		0.25		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Setup Time	100		100		ns
t_R	Inputs Rise Time[1]		0.3		0.3	µs
t_F	Inputs Fall Time[1]		300		100	ns
$t_{SU.STO}$	Stop Setup Time	0.6		.25		µs
t_{DH}	Data Out Hold Time	50		50		ns
t_{WR}	Write Cycle Time		5		5	ms
Endurance[1]	3.3V, +25°C, Page Mode	1,000,000				Write Cycles

Note: 1. This parameter is ensured by characterization only.

6. Device Operation

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a Start or Stop condition as defined below.

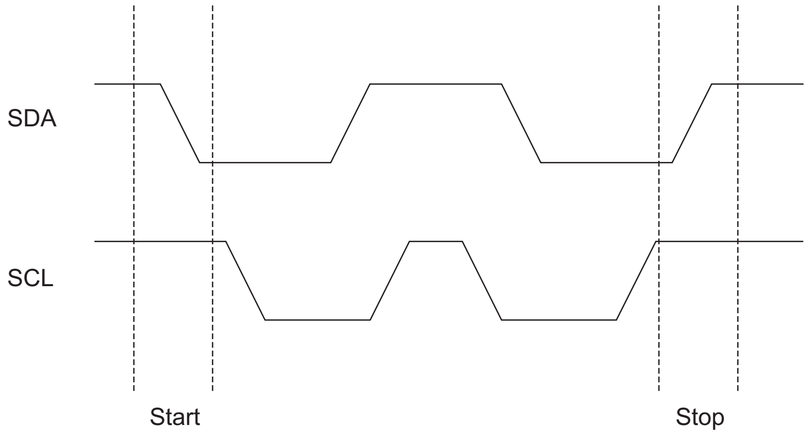
Figure 6-1. Data Validity



Start Condition: A high-to-low transition of SDA with SCL high is a Start condition which must precede any other command.

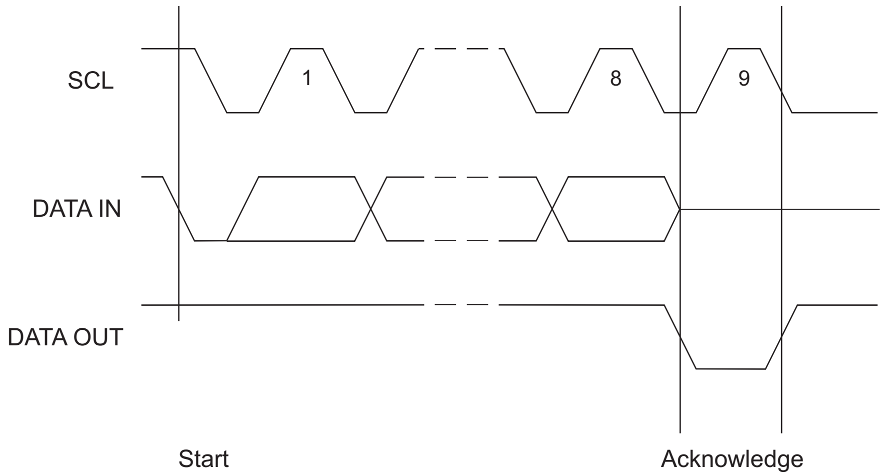
Stop Condition: A low-to-high transition of SDA with SCL high is a Stop condition. After a read sequence, the Stop command will place the EEPROM in a standby power mode.

Figure 6-2. Start and Stop Definition



Acknowledge: All addresses and data words are serially transmitted to and from the EEPROM in eight bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

Figure 6-3. Output Acknowledge



Standby Mode: The Atmel AT24C04/08C features a low-power standby mode which is enabled:

- Upon power-up.
- After the receipt of the Stop condition and the completion of any internal operations.

2-wire Software Reset: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by following these steps:

1. Create a Start condition (if possible).
2. Clock nine cycles.
3. Create another Start condition followed by Stop condition as shown below.

The device should be ready for the next communication after above steps have been completed. In the event that the device is still non-responsive or remains active on the SDA bus, a power cycle must be used to reset the device.

Figure 6-4. Software Reset

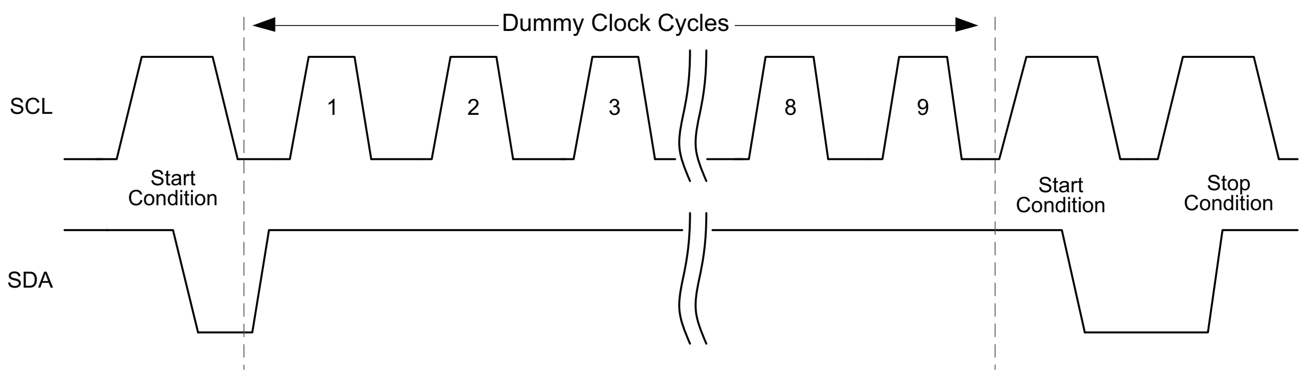


Figure 6-5. Bus Timing

SCL: Serial Clock, SDA: Serial Data I/O

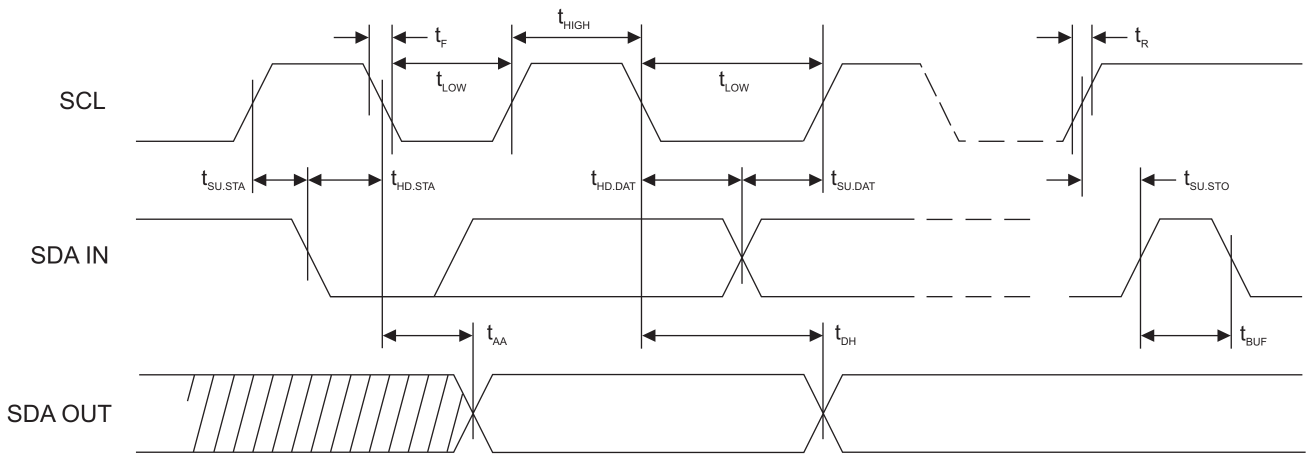
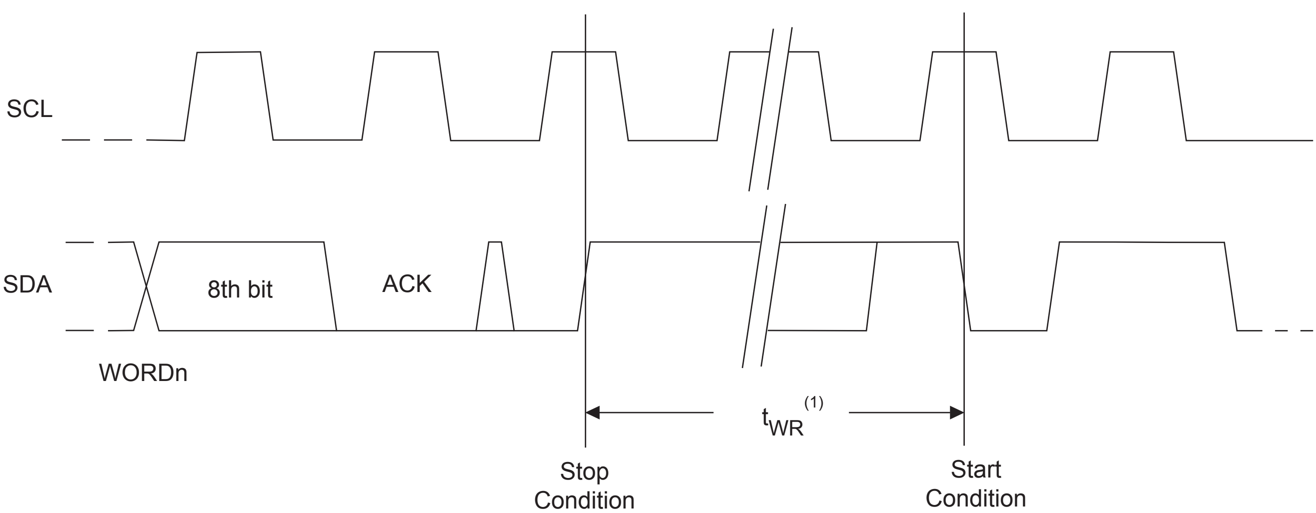


Figure 6-6. Write Cycle Timing

SCL: Serial Clock, SDA: Serial Data I/O



Notes: 1. The write cycle time t_{WR} is the time from a valid Stop condition of a write sequence to the end of the internal clear/write cycle.

7. Device Addressing

Standard EEPROM Access: The 4K and 8K EEPROM device requires an 8-bit device address word following a start condition to enable the chip for a read or write operation. The device address word consists of a mandatory "`1010`" (0xA) sequence for the first four Most Significant Bits (MSB) as shown in Figure 7-1. This is common to all the EEPROM devices.

The 4K EEPROM only uses the A2 and A1 device address bits with the third bit being a memory page address bit. The two device address bits must compare to their corresponding hard-wired input pins. The A_0 pin is no connect.

The 8K EEPROM only uses the A2 device address bit with the next two bits being for memory page addressing. The A2 address bit must compare to its corresponding hard-wired input pin. The A_1 and A_0 pins are no connect.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the chip will return to a standby state.

For the SOT23 package offering, the 4K EEPROM software A2 and A1 bits in the device address word must be set to zero to properly communicate. The 8K EEPROM software A2 bit in the device address word must be set to zero to properly communicate.

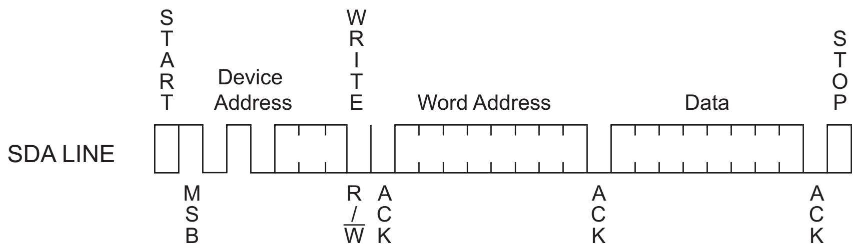
Figure 7-1. Device Address

Density	Access Area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
4K	EEPROM	1	0	1	0	A_2	A_1	P0	$R/\overline{W}$
8K	EEPROM	1	0	1	0	A_2	P1	P0	$R/\overline{W}$
		MSB							LSB

8. Write Operations

Byte Write: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a Stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete.

Figure 8-1. Byte Write

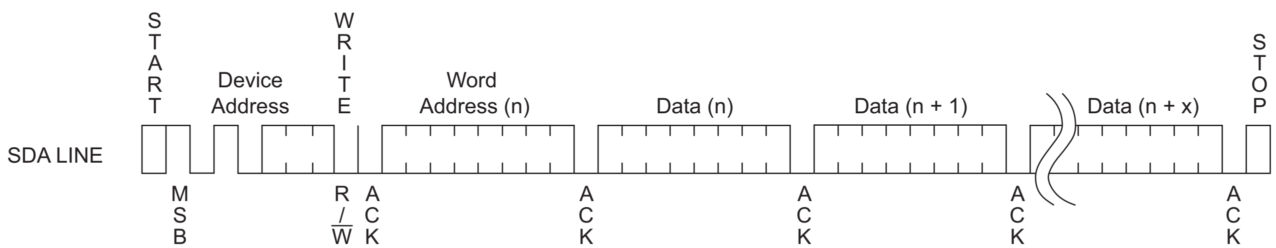


Page Write: The 4K and 8K EEPROM devices are capable of a 16-byte Page Write.

A Page Write is initiated in the same way as a Byte Write, but the microcontroller does not send a Stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to fifteen more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the Page Write sequence with a Stop condition.

The data word address lower four bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 16 data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

Figure 8-2. Page Write



Acknowledge Polling: Once the internally timed write cycle has started and the EEPROM inputs are disabled, Acknowledge Polling can be initiated. This involves sending a Start condition followed by the device address word. The Read/Write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

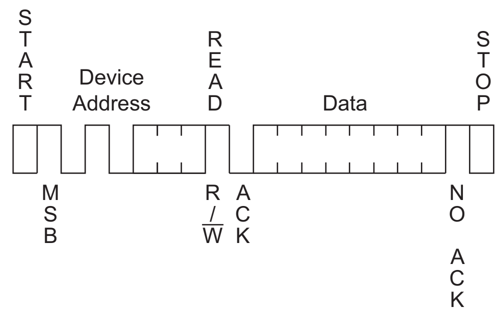
9. Read Operations

Read operations are initiated in the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: Current Address Read, Random Address Read, and Sequential Read.

Current Address Read: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll-over during read is from the last byte of the last memory page to the first byte of the first page. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

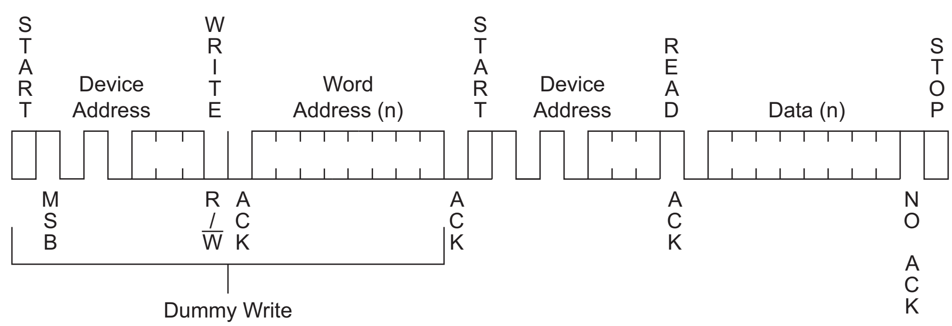
Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition.

Figure 9-1. Current Address Read



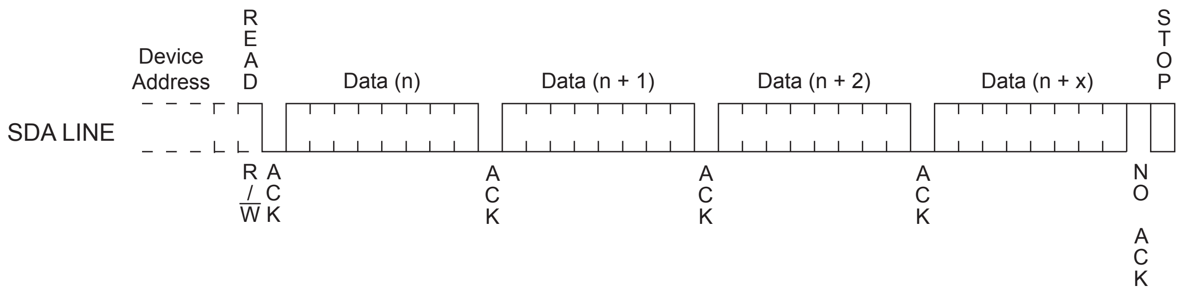
Random Read: A random read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a Current Address Read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition.

Figure 9-2. Random Read



Sequential Read: Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with an Acknowledge. As long as the EEPROM receives an Acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a zero but does generate a following Stop condition.

Figure 9-3. Sequential Read



10. Ordering Code Detail

A T 2 4 C 0 4 C - S S H M - B

Atmel Designator

Product Family
24C = Standard Serial EEPROM

Device Density
04 = 4K
08 = 8K

Device Revision

Shipping Carrier Option
B or blank = Bulk (Tubes)
T = Tape and Reel, Standard Quantity Option
E = Tape and Reel, Expanded Quantity Option

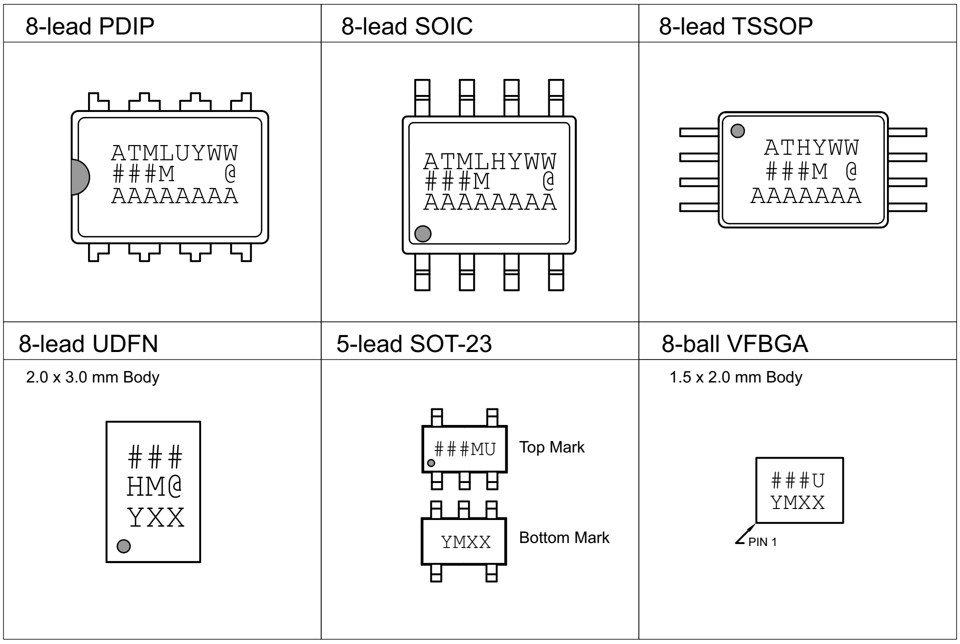
Operating Voltage
M = 1.7V to 5.5V

Package Device Grade or Wafer/Die Thickness
H = Green, NiPdAu Lead Finish, Industrial Temperature Range (-40˚C to +85˚C)
U = Green, Matte Sn Lead Finish, Industrial Temperature Range (-40˚C to +85˚C)
11 = 11mil Wafer Thickness

Package Option
P = PDIP
SS = JEDEC SOIC
X = TSSOP
MA = UDFN
ST = SOT23
C = VFBGA
WWU = Wafer Unsawn

11. Product Markings

AT24C04C and AT24C08C: Package Marking Information



Note 1: ● designates pin 1

Note 2: Package drawings are not to scale

Catalog Number Truncation	
AT24C04C	Truncation Code ###: 04C
AT24C08C	Truncation Code ###: 08C

Date Codes			**Voltages**
Y = Year 2: 2012 6: 2016 3: 2013 7: 2017 4: 2014 8: 2018 5: 2015 9: 2019	M = Month A: January B: February ... L: December	WW = Work Week of Assembly 02: Week 2 04: Week 4 ... 52: Week 52	M: 1.7V min

Country of Assembly	**Lot Number**	**Grade/Lead Finish Material**
@ = Country of Assembly	AAA...A = Atmel Wafer Lot Number	U: Industrial/Matte Tin H: Industrial/NiPdAu

Trace Code	**Atmel Truncation**
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ	AT: Atmel ATM: Atmel ATML: Atmel

5/01/12

	TITLE	DRAWING NO.	REV.
Atmel Package Mark Contact: DL-CSO-Assy_eng@atmel.com	24C04-08CSM, AT24C04C and AT24C08C Package Marking Information	24C04-08CSM	B

12. Ordering Information

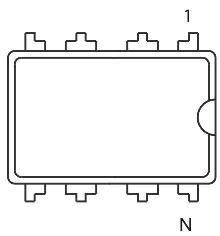
Atmel Ordering Code	Lead Finish	Package	Delivery Information Form	Delivery Information Quantity	Operation Range
AT24C04C-SSHM-B	NiPdAu (Lead-free/Halogen-free)	8S1	Bulk (Tubes)	100 per Tube	Industrial Temperature (-40°C to 85°C)
AT24C04C-SSHM-T			Tape and Reel	4,000 per Reel	
AT24C04C-XHM-B		8X	Bulk (Tubes)	100 per Tube	
AT24C04C-XHM-T			Tape and Reel	5,000 per Reel	
AT24C04C-MAHM-T		8MA2	Tape and Reel	5,000 per Reel	
AT24C04C-MAHM-E			Tape and Reel	15,000 per Reel	
AT24C04C-PUM	Matte Tin (Lead-free/Halogen-free)	8P3	Bulk (Tubes)	50 per Tube	
AT24C04C-STUM-T		5TS1	Tape and Reel	5,000 per Reel	
AT24C04C-CUM-T	SnAgCu Ball (Lead-free/Halogen-free)	8U3-1	Tape and Reel	5,000 per Reel	
AT24C04C-WWU11M[1]	N/A	Wafer Sale	Note 1		
AT24C08C-SSHM-B	NiPdAu (Lead-free/Halogen-free)	8S1	Bulk (Tubes)	100 per Tube	Industrial Temperature (-40°C to 85°C)
AT24C08C-SSHM-T			Tape and Reel	4,000 per Reel	
AT24C08C-XHM-B		8X	Bulk (Tubes)	100 per Tube	
AT24C08C-XHM-T			Tape and Reel	5,000 per Reel	
AT24C08C-MAHM-T		8MA2	Tape and Reel	5,000 per Reel	
AT24C08C-MAHM-E			Tape and Reel	15,000 per Reel	
AT24C08C-PUM	Matte Tin (Lead-free/Halogen-free)	8P3	Bulk (Tubes)	50 per Tube	
AT24C08C-STUM-T		5TS1	Tape and Reel	5,000 per Reel	
AT24C08C-CUM-T	SnAgCu Ball (Lead-free/Halogen-free)	8U3-1	Tape and Reel	5,000 per Reel	
AT24C08C-WWU11M[1]	N/A	Wafer Sale	Note 1		

Note: 1. For Wafer sales, please contact Atmel Sales.

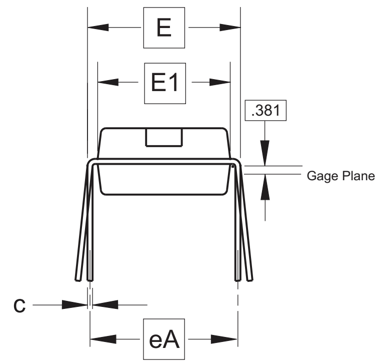
Package Type	
8P3	8-lead, 0.300" wide, Plastic Dual Inline Package (PDIP)
8S1	8-lead, 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8X	8-lead, 4.4mm body, Plastic Thin Shrink Small Outline Package (TSSOP)
8MA2	8-pad, 2.00mm x 3.00mm body, 0.50mm pitch, Plastic Ultra Thin Dual Flat No Lead (UDFN)
5TS1	5-lead, 2.90mm x 1.60mm body, Plastic Thin Shrink Small Outline (SOT23)
8U3-1	8-ball, 1.50mm x 2.00mm body, 0.50mm pitch, Die Ball Grid Array (VFBGA)

13. Packaging Information

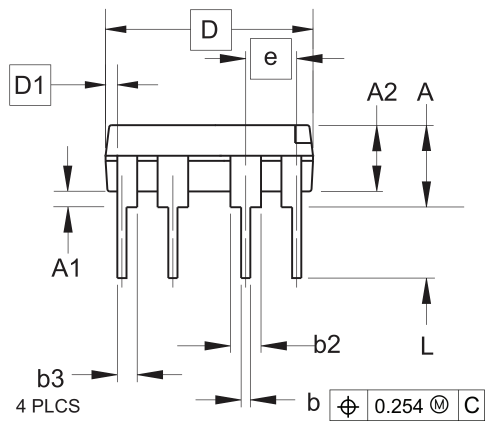
13.1 8P3 — 8-lead PDIP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

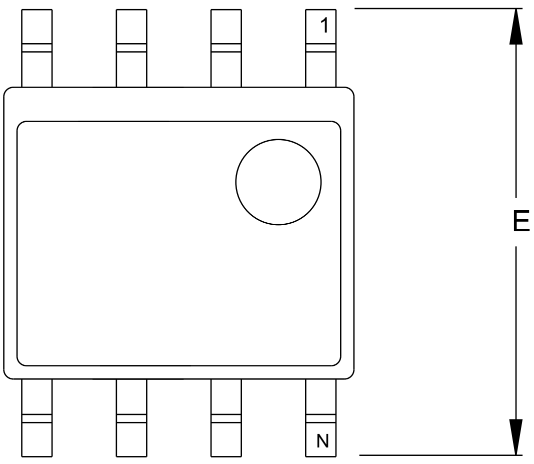
SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	5.334	2
A1	0.381	-	-	
A2	2.921	3.302	4.953	
b	0.356	0.457	0.559	5
b2	1.143	1.524	1.778	6
b3	0.762	0.991	1.143	6
c	0.203	0.254	0.356	
D	9.017	9.271	10.160	3
D1	0.127	0.000	0.000	3
E	7.620	7.874	8.255	4
E1	6.096	6.350	7.112	3
e	2.540 BSC			
eA	7.620 BSC			4
L	2.921	3.302	3.810	2

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

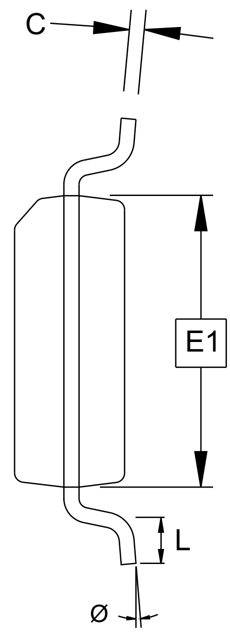
07/31/14

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 8P3, 8-lead, 0.300” Wide Body, Plastic Dual In-line Package (PDIP)	GPC PTC	DRAWING NO. 8P3	REV. E

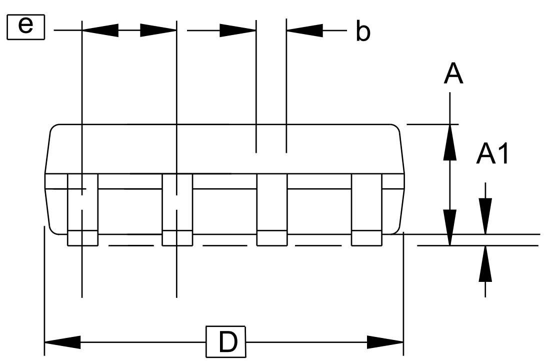
13.2 8S1 — 8-lead JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

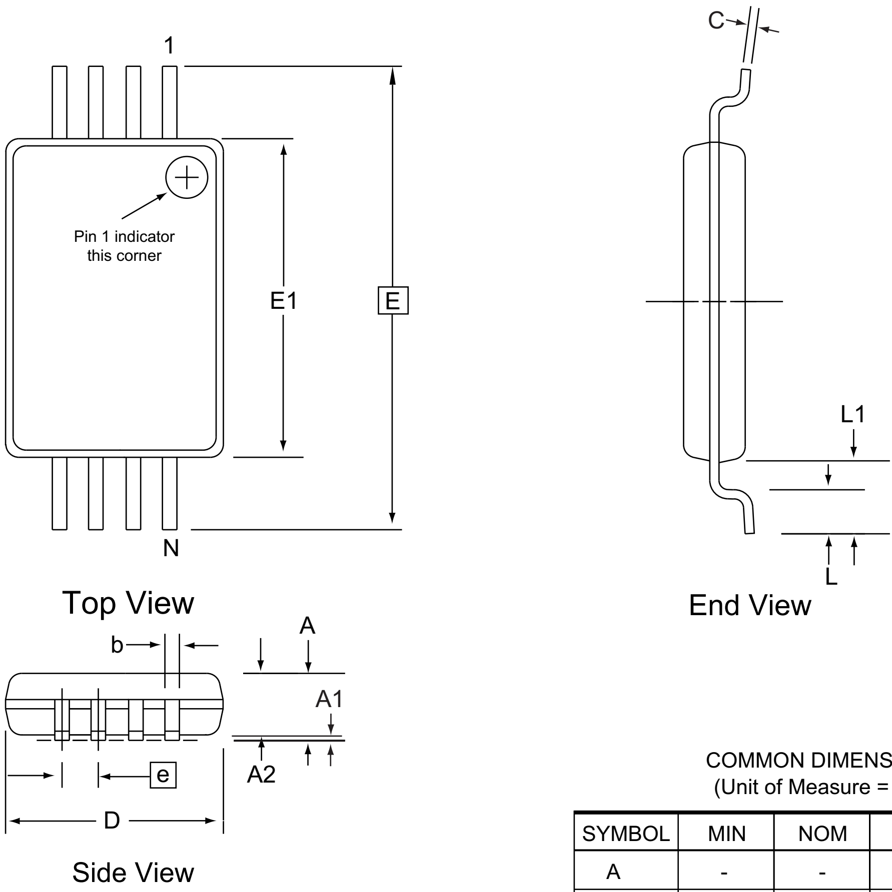
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

6/22/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**GPC** SWB	**DRAWING NO.** 8S1	**REV.** G

13.3 8X — 8-lead TSSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

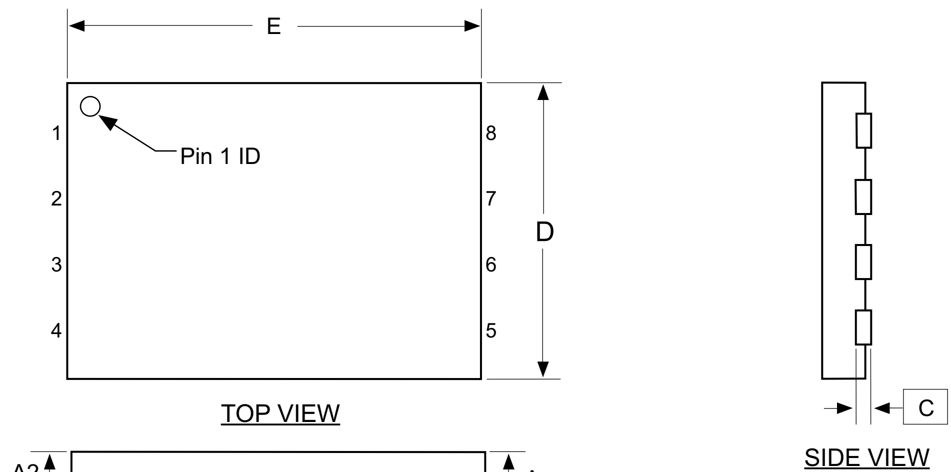
SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.05	-	0.15	
A2	0.80	1.00	1.05	
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
b	0.19	0.25	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		
C	0.09	-	0.20	

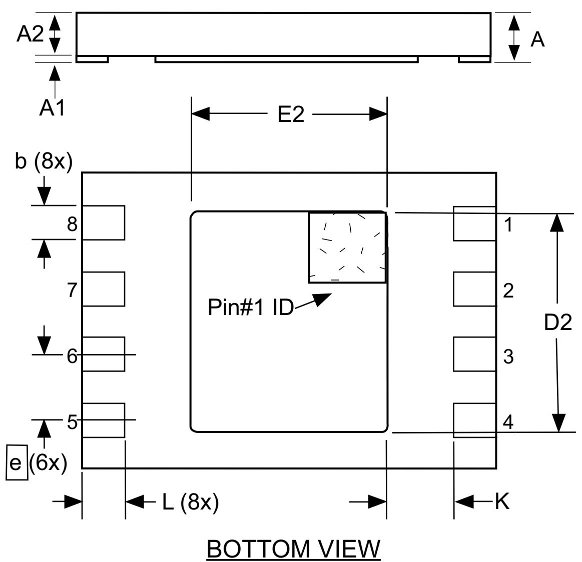
Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

2/27/14

Atmel	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	8X, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	TNR	8X	E

13.4 8MA2 — 8-pad UDFN





Notes:
1. This drawing is for general information only. Refer to Drawing MO-229, for proper dimensions, tolerances, datums, etc.
2. The Pin #1 ID is a laser-marked feature on Top View.
3. Dimensions b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.
4. The Pin #1 ID on the Bottom View is an orientation feature on the thermal pad.

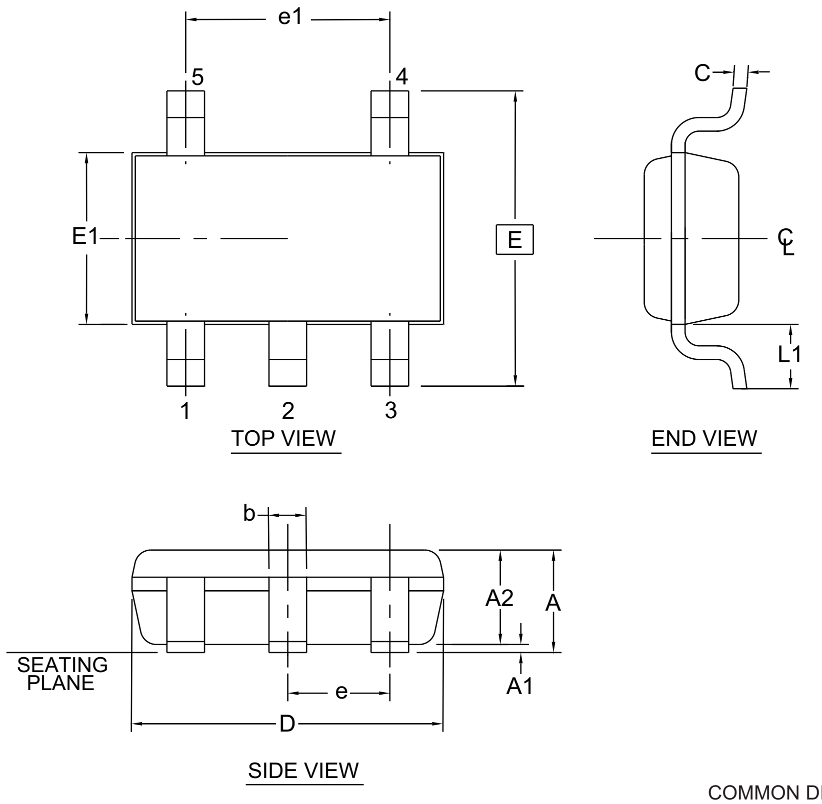
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.50	0.55	0.60	
A1	0.0	0.02	0.05	
A2	-	-	0.55	
D	1.90	2.00	2.10	
D2	1.40	1.50	1.60	
E	2.90	3.00	3.10	
E2	1.20	1.30	1.40	
b	0.18	0.25	0.30	3
C		1.52 REF		
L	0.30	0.35	0.40	
e		0.50 BSC		
K	0.20	-	-	

11/26/14

Atmel	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	8MA2, 8-pad 2 x 3 x 0.6mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat No-Lead Package (UDFN)	YNZ	8MA2	G

13.5 5TS1 — 5-lead SOT23



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.00	
A1	0.00	-	0.10	
A2	0.70	0.90	1.00	
c	0.08	-	0.20	3
D		2.90 BSC		1,2
E		2.80 BSC		1,2
E1		1.60 BSC		1,2
L1		0.60 REF		
e		0.95 BSC		
e1		1.90 BSC		
b	0.30	-	0.50	3,4

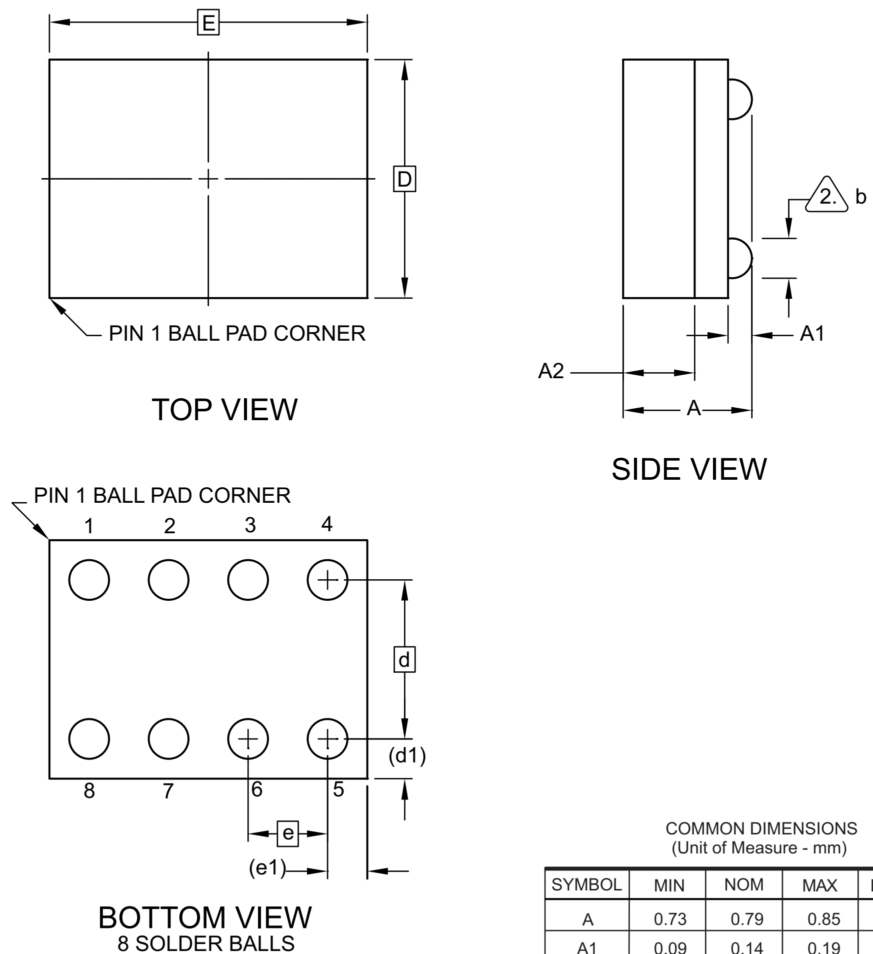
1. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.15 mm per side.
2. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
3. These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.
4. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the "b" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and an adjacent lead shall not be less than 0.07 mm.

This drawing is for general information only. Refer to JEDEC Drawing MO-193, Variation AB for additional information.

5/31/12

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 5TS1, 5-lead 1.60mm Body, Plastic Thin Shrink Small Outline Package (Shrink SOT)	GPC TSZ	DRAWING NO. 5TS1	REV. D

13.6 8U3-1 — 8-ball VFBGA



Notes:

1. This drawing is for general information only.
2. Dimension ‘b’ is measured at maximum solder ball diameter.
3. Solder ball composition shall be 95.5Sn-4.0Ag-.5Cu.

COMMON DIMENSIONS
(Unit of Measure - mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.73	0.79	0.85	
A1	0.09	0.14	0.19	
A2	0.40	0.45	0.50	
b	0.20	0.25	0.30	2
D		1.50 BSC		
E		2.0 BSC		
e		0.50 BSC		
e1		0.25 REF		
d		1.00 BSC		
d1		0.25 REF		

6/11/13

Atmel	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	8U3-1, 8-ball, 1.50mm x 2.00mm body, 0.50mm pitch, Very Thin, Fine-Pitch Ball Grid Array Package (VFBGA)	GXU	8U3-1	F

14. Revision History

Doc. Rev.	Date	Comments
8787E	01/2015	Add the UDFN expanded quantity options and update the ordering information section. No change in functional or electrical specification. Update the 8P3, 8X, 8MA2, and 8U3-1 package outline drawings and the disclaimer page.
8787D	04/2013	In the Page Write description, correct from eight to 16 data words. Update ordering code table, footers, and disclaimer page.
8787C	07/2012	Correct ordering codes: - AT24C04C-WWU11, Die Sale to AT24C04C-WWU11M, Wafer Sale. - AT24C08C-WWU11, Die Sale to AT24C08C-WWU11M, Wafer Sale. Remove WDT from ordering code detail. Update Atmel logos and disclaimer page.
8787B	05/2012	Remove preliminary status. Remove A_0 signal from the block diagram. I_{SB2} parameter measured at 5.5V. In AC Characteristics table, changed 1.7V, 2.5V, 2.7V to 1.7 and 5.0V to 2.5V, 2.7V, 5.0V. Increase t_I maximum value from 50ns to 100ns. Endurance parameter is studied at 3.3V, to +25°C, Page mode. Remove Serial Number Read from read operations. Update product markings. Update 8X and 8U3-1 package drawings. Update template.
8787A	10/2011	Initial document release.

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